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A wireless transceiver comprises a digital to analog converter having an input for receiving a digital representation of a direct sequence spread spectrum signal and having an analog output. A bandpass or lowpass filter has an input coupled to the analog output of the digital to analog converter and has a filtered output. An adder has a first input coupled to the filtered output and a second input coupled to a loop control voltage generated by a phase lock loop. The adder produces a summed output. A VCO integrated into the phase lock loop has a control input coupled to the summed output. An RF output of the VCO produces a continuous phase frequency shift keyed spread spectrum signal in response to the digital representation of the direct sequence spread spectrum signal.

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**DIRECT CONVERSION TIME DIVISION DUPLEX RADIO, DIRECT
SEQUENCE SPREAD SPECTRUM CORDLESS TELEPHONE**

Background of the Invention

I. Field of the Invention

5 The invention relates generally to communications. More specifically, the invention relates to wireless telecommunications.

II. Description of the Related Art

10 The cordless telephone has become a popular consumer good. The cordless telephone allows a user to untether himself from a wired connection to his local telephone line. Typically, a cordless telephone is comprised of two units: a base unit and a handset. The base unit connects to the public switched telephone network typically using a standard RJ-11 connector. The base unit provides a wireless connection to a handset. The handset is capable of receiving and transmitting signals over a wireless link to the base unit. The use of the wireless link allows the handset to communicate with the base unit.

15 The consumer cordless telephone market is a competitive market. Cordless telephone products on the market compete with one another based on audio quality, reliability over various operating conditions, privacy, battery life, the physical range over which the device operates, and cost. In order to achieve favorable measures of these characteristics, the wireless interface which connects the handset to the base unit must operate efficiently.

20 One efficient way which cordless telephones operate is called time division duplex (TDD). In time division duplex, the base unit and the handset alternately transmit such that the units do not transmit at the same time. In a time division duplex system, the same frequency band can be used for both transmission and reception. By using time division duplex, the transmit and receive circuitry within each unit can share common components. In addition, each unit requires less internal isolation between the transmit and receive circuitry. For these reasons, a cordless telephone which operates using time division duplex can be cheaper, more reliable and yet produce higher quality audio signals than a full duplex unit. Even though the wireless link operates using time division duplex, audio compression techniques are used to provide concurrent bi-directional audio communication to the user. Therefore, even though the wireless link signals are time division duplex, the end user perceives simultaneous bi-directional audio communication.

25 Another technique used in cordless telephones is direct sequence spread spectrum (DSSS). Spread spectrum signals used for the transmission of digital information are distinguished by the characteristic that their bandwidth is much greater than their information rate in bits per second. The large redundancy introduced by spread spectrum operation can be used to overcome severe levels of interference. In addition, spread spectrum can be used to introduce pseudo-randomness into the signal. Transmission signals spread with a pseudo-random code appear to be random noise and are difficult to demodulate by receivers other than the intended receiver. In this way, a system which uses direct sequence spread spectrum is less vulnerable to accidental or deliberate reception by a third party. In this way, direct sequence spread spectrum, in conjunction with a scrambling scheme, provides a significant element of privacy in the communications channel.

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In a direct sequence spread spectrum system, data bits are modulated with a spreading sequence before transmission. Each bit of information is modulated with a series of chips from the spreading sequence. The ratio of the number of chips per bit defines the coding gain. A greater number of chips per bit creates a greater immunity to noise and other interference. For example, in one common cordless telephone spreading technique, each information bit is modulated with a 12 bit spreading code. Because a cordless telephone using direct sequence spread spectrum has some immunity to noise and other interference, the cordless telephone handset may transmit a very low output power. By decreasing the transmit power, the battery life of the handset is increased.

In a typical embodiment, the spreading code contains an even number of one's and zero's. In this way, the energy of the spread spectrum signal is minimized at and close to 0 Hz. For this reason, a baseband spread signal may be subjected to highpass or bandpass filtering with little effect on the information content. In a system in which each information bit is modulated with a 12 bit spreading code, a preferred spreading code can be chosen by examination of the spectral content of each possible 12 bit sequence which is comprised of six 0's and six 1's.

Prior to application of the spreading code to the information bit stream, the information bits may undergo a series of digital operations which further increase the performance of the system. For example, the information bits may undergo differential encoding in order to be more intolerant to an incorrect phase lock in the receiving unit phase locked loop (PLL). The information bits may be scrambled using a long scrambling sequence in order to further decrease the vulnerability of the system to interception.

Conventional cordless telephones utilizing direct sequence spread spectrum coding also use binary phase shift keying (BPSK). In a phase shift keyed system, information is carried in the phase of the signal. For example, in Figure 1A, the binary sequence 1 0 1 1 0 is represented as a series of positive and negative voltage levels. In Figure 1B, the same sequence has been phase shift keyed modulated. In Figure 1B, two different phases are used to denote the two different digital values. Note that whenever the sequence transitions from a "1" to a "0" or from a "0" to a "1", the phase of the signal in Figure 1B transitions. Such a system is referred to as a BPSK system.

Figure 2 is a block diagram showing a prior art BPSK architecture. This architecture may be used by both the base unit and handset. The baseband spread spectrum signal is produced by a digital portion of the architecture which is not shown in Figure 2. The digital spread spectrum waveform is converted to a baseband analog signal by a one bit digital-to-analog converter (DAC) 62. The baseband signal is then amplified by a baseband amplifier 60. After amplification, the signal is passed through bandpass filter 58. The bandpass filter 58 is necessary because the baseband spread spectrum signal contains higher order harmonics which are removed before transmission in order to avoid transmitting out of band energy. In addition, the bandpass filter 58 attenuates signal energy at frequencies at or near 0 Hz. Attenuation of the low frequency components of the baseband signal aids in suppression of the radio frequency (RF) carrier frequency component of the radio output.

The filtered output of the bandpass filter 58 is modulated with an RF carrier by a mixer 56. The RF carrier is generated by a phase lock loop comprised of a voltage control oscillator (VCO) 44, a lowpass filter 46 and a frequency mixer/phase detector 48. During operation, the mixer/phase detector 48 is programmed by the digital architecture to

control the VCO 44 to generate an RF sinusoidal signal at the selected wireless link center frequency. The signal produced by the VCO 44 is applied to the mixer 56 such that the output of the mixer 56 is a BPSK waveform at the desired RF transmit frequency.

The RF BPSK waveform is amplified by an amplifier 54. In addition, the BPSK waveform is amplified by a variable gain power amplifier 50. The gain of the power amplifier 50 is set based upon a transmit power level indication received from the digital architecture and converted to usable form by a power amplifier level control unit 52. The gain of the power amplifier 50 at the transmitter may be decreased as the path loss between the handset and base unit is decreased in order to conserve power. During a transmission period of the time division duplex operation, an RF switch 22 connects the output of the power amplifier 50 to a radio frequency lowpass filter 20. The output of the lowpass filter 20 is transmitted to the receiving unit over an antenna.

During a reception period of the time division duplex operation, a receive signal passes through the lowpass filter 20. The radio frequency switch 22 connects the output of the lowpass filter 20 to an RF bandpass filter 24. The output of the bandpass filter 24 is passed to a variable gain low noise amplifier 26. The gain of the low noise amplifier 26 is selected by an LNA gain level indication generated by the digital architecture. The gain of the low noise amplifier is decreased as the path loss between the base unit and the handset decreases in order to avoid saturation of the receive circuitry. In order to discern the phase of the received signal at the baseband, the received RF signal is down converted using an in-phase and quadrature component of the RF signal produced by the phase lock loop. The RF signal produced by the phase lock loop is shifted by 90 degrees by a phase shifter 42 before use in the quadrature receive path. The in-phase and quadrature components are applied to the mixers 28A and 28B respectively. The output of the mixers 28A and 28B are passed to bandpass filters 30A and 30B, respectively. The output of bandpass filters 30A and 30B are passed to variable gain amplifiers 32A and 32B respectively. The gain of the variable gain amplifiers 32A and 32B is set by a baseband gain level indication received from the digital architecture to control the signal level supplied to subsequent components. The output of the variable gain amplifiers 32A and 32B is converted to a digital representation by analog-to-digital converters (ADCs) 34A and 34B.

The output of ADCs 34A and 34B is sent to matched filters 38A and 38B via a phase rotator 36. The phase rotator 36 attempts to compensate for any frequency offsets affecting the received baseband signal. Although both the transmitting and receiving units have a PLL, the carrier signal produced by the receiving unit is never exactly the same as the carrier signal produced by the transmitting unit due to injected noise, reference frequency variations and other sources of errors. Any difference between the transmitter and receiver carrier signals modulates the resulting baseband signal produced by the receiving unit. The phase rotator 36 attempts to detect and correct for errors due to frequency and phase offsets which modulate the baseband signal.

The matched filters 38A and 38B perform the despreading functions. The despreading function removes the direct sequence spread spectrum modulation from the received signal. The outputs of the matched filters 36A and 36B is input into a BPSK demodulator 40. The BPSK demodulator 40 uses the amplitude of the output of each

matched filter 38A and 38B in order to recover the transmitted information bits from the received signal. A differential decoding stage may also be used if the information bits have been differentially encoded at the transmitter.

When BPSK modulation is used in a spread spectrum system, a mixer is used to modulate the baseband spread spectrum signal onto an RF carrier suitable for transmission over the wireless link. The process of mixing onto an RF carrier can increase the size, cost and power consumption of the cordless telephone system.

In addition, the demodulation of a BPSK signal requires the detection of the phase of the received baseband signal. A system which requires phase detection is sensitive to VCO errors. Errors in the VCO may be introduced by many mechanisms such as injection of radiated RF noise and conduction of noise on the DC supply voltage. In addition, during a transmit period, leakage of the RF transmitted signal into the PLL may cause the frequency of the VCO output signal to diverge from the desired value through a phenomenon termed "VCO pulling." VCO pulling causes a frequency offset in the transmitted signal which modulates the recovered baseband signal at the receiving unit. Even when the transmit period ends and the receive period begins, there may be an initial time interval during which the PLL reacquires frequency lock at the desired frequency to overcome the effects of VCO pulling. During the reacquisition time interval, the received baseband signal continues to be effected by the VCO errors.

Any error in the frequency of the RF signal generated by the VCO within the receiver relative to the VCO within the transmitter causes the received BPSK signal to have an amplitude modulation at a frequency equal to the VCO cumulative errors. The presence of amplitude modulation may cause bit errors and, if the modulation becomes severe, the receiver may fail to recover the transmitted information.

Therefore, there has been a long felt need to have an alternate modulation technique and architecture which overcomes the problems and inefficiencies encountered in a direct conversion radio, DSSS BPSK wireless communication system.

Summary of the Invention

A cordless telephone incorporates continuous phase, frequency shift keying (CPFSK) modulation to create an efficient RF/analog architecture. A spreading sequence with low spectral energy at or near 0 Hz is used to digitally spread information bits within a digital architecture. The resulting digital sequence is converted to an analog baseband signal. The analog baseband signal is bandpass filtered to further reduce the spectral energy at or near 0 Hz. The resulting signal is called the modulation control signal. The modulation control signal is summed with a control voltage generated by a phase lock loop. The summed result is applied to the control input of a voltage controlled oscillator. The resulting VCO output is amplified and transmitted over the wireless link. The phase lock loop incorporates a lowpass filter which greatly reduces the effect of the modulation control signal on the lock state of the phase lock loop.

Within the receiver architecture, the received RF waveform is converted into in-phase and quadrature baseband components. The in-phase and quadrature baseband signal components are converted to digital form and demodulated. The resulting sequence is despread to produce estimated bit data.

Brief Description of the Drawings

The features, objectives, and advantages of the invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings wherein like parts are identified with like reference numeral throughout and wherein:

5 Figure 1 is a time domain diagram illustrating binary phase shift keying (BPSK) and continuous phase frequency shift keying (CPFSK) modulation waveforms;

 Figure 2 is a block diagram showing a prior art binary phase shift keyed architecture of a handset or base unit; and

10 Figure 3 is a block diagram showing the architecture of a direct conversion radio, time division duplex, direct sequence spread spectrum cordless telephone handset or base unit using continuous phase frequency shift keying.

Detailed Description of the Preferred Embodiment

 In a frequency shift keyed system, digital information is carried in the frequency of the signal. For example, in Figure 1A, the binary sequence 1 0 1 1 0 is represented as a series of positive and negative voltage levels. In Figure 1C, the same sequence has been frequency shift key modulated. In the particular scheme shown in Figure 1C, a digital value of "1" has been represented by a higher frequency than the digital value "0". Also note in Figure 1C that when a transition between a 1 and a 0 occurs, the phase of the signal does not experience an abrupt change but rather a smooth transition from the first frequency to the second frequency is made. Such a system is referred to as a continuous phase frequency shift keyed system.

20 Figure 3 is a block diagram showing the architecture of a direct conversion radio, time division duplex, direct sequence spread spectrum cordless telephone handset or base unit. A digital spread spectrum signal such as the one shown in Figure 1A, is generated in a digital architecture not shown in Figure 3. The digital spread spectrum signal is applied to a one bit digital to analog converter (DAC) 112. It is helpful to note that the output of the DAC 112 is not a baseband representation of the spectrum for transmission (as shown, for example, in Figure 1C) but is instead an analog representation of the digital signal. In the most general embodiment, a DAC with more than one input bit may be used. The output of the DAC 112 is applied to an analog amplifier 110. The output of the amplifier 110 is applied to a bandpass filter 108 to produce the modulation control signal. The analog representation of the digital spread spectrum signal may be filtered by the bandpass filter 108 (or with a highpass filter) with minimal loss of information in the transmitted signal because the data has been modulated with a spreading code chosen to minimize the information content at frequencies at or near 0 Hz. The effect of the combination of the chosen spreading code and the bandpass filter 108 is that the low frequency energy of the modulation control signal is minimal.

30 The modulation control signal is injected into the control loop of a phase lock loop comprised of a voltage control oscillator (VCO) 92, a lowpass loop filter 94 and a frequency mixer/phase detector 96. During operation, the mixer/phase detector 96 is programmed by the digital architecture to control the VCO 92 to generate an RF signal at the selected wireless link center frequency. In the absence of the modulation control signal, the RF output of the VCO 92 is locked to the phase of a reference signal which is also input into mixer/phase detector 96.

The modulation control signal is summed with the control voltage of the VCO 92 by an adder 106. The adder 106 may be one of a variety well-known devices including a simple resistive network. Because the modulation control signal has a minimal low frequency component, the effects of injecting the modulation control signal into the loop is minimal. The high frequency components of the modulation signal index are filtered out by the lowpass filter 94 so that the PLL does not react to the high frequency components.

The RF signal at the output of VCO 92 ($v_o(t)$) is mathematically related to the modulation control signal ($v_i(t)$) by the following equation:

$$v_o(t) = \cos \left(2\pi f_0 t + \int_0^t v_i(\tau) d\tau \right)$$

where f_0 is the frequency at which the PLL is programmed to operate. The modulation control signal, $v_i(t)$, is a CPFSK modulation signal at the output of bandpass filter 108. Comparing Figure 3 to Figure 2 reveals that the VCO 92 is directly modulated with the modulation control signal, thereby eliminating the use of a discrete mixer (such as the mixer 56 in Figure 2) for upconversion of an analog baseband signal to an RF frequency output signal. Elimination of a separate upconversion process decreases the size, cost and power consumption of the system.

The output of the VCO 92 is amplified by an amplifier 104. In addition, the RF transmit signal is amplified in a variable gain power amplifier 100. The gain of the variable gain power amplifier 100 is set according to a transmit power level indication received from the digital architecture and converted to usable form by the power amplifier level control unit 102. The output of the variable gain power amplifier 100 is passed to an RF switch 72. During the transmission period of the time division duplex operation, the RF switch 72 connects the output of the variable gain power amplifier 100 to a lowpass filter 70, according to a transmit/receive select indication received from the digital architecture. The output of lowpass filter 70 is transmitted with an antenna.

During the receive periods of the time division duplex operation, RF signals are received from an antenna and passed through the lowpass filter 70. The RF switch 72 connects the output of lowpass filter 70 to the input of a bandpass filter 74. The output of the bandpass filter 74 is connected to a variable gain low noise amplifier 76. The gain of the variable gain low noise amplifier 76 is set by an LNA gain level indication received from the digital architecture. The gain of the variable gain low noise amplifier 76 may be decreased as the path loss between the handset and base unit decreases in order to avoid overdriving subsequent stages.

In order to discern the frequency of the received RF signal, the output of the low noise amplifier 76 is down converted into in-phase and quadrature-phase components. The output of the VCO 92 is input into a phase shifter 90 such that an in-phase and quadrature component of the output of the VCO 92 is applied respectively to mixers 78A and 78B. During a receive period, the spread spectrum input to the adder 106 is not present, therefore, the output of the VCO 92 is simply an unmodulated RF sinusoidal signal. The output of the mixers 78A and 78B are applied to bandpass filters 80A and 80B respectively. The outputs of the bandpass filters 80A and 80B are applied to variable gain amplifiers 82A and 82B respectively. The gain of the variable gain amplifiers 82A and 82B is set by a receive baseband gain level indication received from the digital architecture. The receive baseband digital gain indication sets

the output level of the gain of the amplifiers 82A and 82B to a proper level for input into subsequent processing stages. The output of the amplifier 82A and 82B is converted to a digital representation by analog-to-digital converters (ADCs) 84A and 84B respectively. The output of the ADCs 84A and 84B are sent to an FSK demodulator 86. The FSK demodulator 86 estimates the phase transition between successive chips by calculating the phase angle
5 between them. In a binary CPFSK modulation scheme, only 2 allowed phase transitions occur: a transition from the higher frequency to the lower frequency and a transition from the lower frequency to the higher frequency. Estimating the sequence of phase transitions between adjacent chips effectively provides an estimate of the digital value of each chip in the received chip sequence. The estimated chip data is sent to a matched filter 88 which removes the effect of the spreading code and, thereby, provides an estimate of the transmitted information bits.

10 One advantage of the CPFSK architecture of Figure 3 over the BPSK architecture of Figure 2 is that the architecture of Figure 3 is less sensitive to VCO errors. In a BPSK system, the phase of the received signal is directly estimated. Any offset in the receiver VCO frequency relative to the transmitter VCO frequency modulates the baseband received BPSK signal at the offset frequency. Unless compensation for the undesired modulation (such as the phase rotator 36 in Figure 2) is included in the demodulation process, the undesired modulation results in errors in
15 recovering the transmitted data. On the other hand, in a CPFSK system the demodulator uses the phase transition as the signal changes continuously from one frequency state to another. The measurement of phase transition from one frequency to another is not effected by offsets in the receiver VCO frequency relative to the transmitter VCO frequency because the differential phase transition remains the same even if the VCO frequencies are offset.

VCO errors and offsets may be generated by a variety of phenomenon. For example, any low frequency noise
20 on the DC power supply voltage line for the VCO may modulate the phase of the output of the VCO. In addition, the VCO output frequency may be dependent upon the impedance level which the VCO is driving. Therefore, if the impedance level seen by the VCO 92 changes when a transition between transmission and reception in the time division duplex operation occurs, the output frequency of the VCO may experience phase errors during the transition. Because the architecture of Figure 3 uses a direct modulation and conversion scheme to create the digital transmit
25 signal, the signal at the output of the variable gain power amplifier 100 is a delayed version of the output of the VCO 92. For this reason, any RF leakage which occurs from the variable gain power amplifier 100 back to the phase lock loop is much less likely to effect convergence to the desired frequency than in the configuration shown in Figure 2 where the output of the VCO 44 is unmodulated as compared to the modulated output of the variable gain power amplifier 50. In this way, VCO errors are reduced and the sensitivity of the radio to VCO errors is reduced thereby
30 eliminating the need for a compensation component (such as the phase rotator 36 of Figure 2.) For these reasons, the performance of the FSK system is increased and the size, cost and power consumption of the base unit and handset in the FSK system are decreased.

Another advantage of the CPFSK architecture in Figure 3 over the BPSK architecture in Figure 2 is that only one matched filter 88 is required as opposed to two matched filters 38A and 38B in the BPSK architecture. A typical
35 matched filter is implemented using digital circuitry in an ASIC. Elimination of a matched filter reduces the size, cost

and power consumption of the base unit and handset. The use of a single matched filter is possible in the FSK architecture because demodulation is performed at the chip level rather than the bit level. In this way, the in-phase and quadrature components have been combined into a single bit stream before the despreading process. By comparison, the BPSK architecture does not lend itself to the use of a single matched filter because the matched filtering is performed on both an in-phase and a quadrature-phase component of the complex signal.

Although a variety of modulation characteristics can be applied to the general architecture shown in Figure 3, in one embodiment, the RF carrier frequency output by the VCO for both transmission and receive is within the range of 902-928 megahertz (MHz). The CPFSK modulated frequencies may be offset from the RF carrier frequency such as by ± 480 kilohertz (kHz). The direct sequence spread spectrum characteristics may also take on a variety of values. In one example, the information bit rate is 100 kilobits per second and the chip rate is 1.2 megachips per second. Each bit may be modulated a 12 chip spreading sequence.

The invention was illustrated herein with respect to a cordless telephone environment. However, the invention is broadly applicable to a number of environments which incorporate a wireless link.

The invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments is to be considered in all respects only as illustrative and not restrictive and the scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning of equivalency of the claims are to be embraced within their scope.

WHAT IS CLAIMED IS:

1. A wireless transceiver comprising:
a digital to analog converter having an input for receiving a digital representation of a direct
sequence spread spectrum signal and having an analog output;
5 an analog filter which attenuates energy at or near 0 Hz, said analog filter having an input coupled
to said analog output of said digital to analog converter and having a filtered output;
an adder having a first input coupled to said filtered output, having a second input coupled to a loop
control voltage generated by a phase lock loop and having a summed output; and
a VCO having a control input coupled to said summed output and having an RF output, wherein said
10 RF output is configured to produce a continuous phase frequency shift keyed spread spectrum signal in
response to said summed output.
2. The wireless transceiver of Claim 1, wherein said VCO is integrated into said phase lock loop.
3. The wireless system of Claim 1 wherein said direct sequence spread spectrum signal is spread with
a spreading sequence which has a very low spectral energy at and near to 0 Hz.
- 15 4. The wireless system of Claim 1 wherein said phase lock loop incorporates a lowpass filter which
attenuates energy at at least some of the frequencies passed by said analog filter.
5. A method of generating a radio frequency spread spectrum signal comprising the steps of:
bandpass or lowpass filtering an analog representation of a digital direct sequence spread spectrum
waveform to produce a modulation control signal;
20 summing said modulation control signal with a loop control signal to create a summed control
signal;
applying said summed control signal to a voltage controlled oscillator to create a modulated RF
output;
comparing said modulated RF output to a reference frequency input to create a phase error signal;
25 and
lowpass filtering said phase error signal to produce said loop control signal in order to reduce the
effects of said modulation control signal on said loop control signal.
6. The method of generating a radio frequency spread spectrum signal of Claim 5 further comprising
the step of generating said digital direct sequence spread spectrum waveform using a spreading sequence which has a
30 very low spectral energy at or near 0 Hz.
7. A system for generating a radio frequency spread spectrum signal comprising:
means for bandpass or lowpass filtering an analog representation of a digital direct sequence
spread spectrum waveform to produce a modulation control signal;
means for summing said modulation control signal with a loop control signal to create a summed
35 control signal;

means for applying said summed control signal to a voltage controlled oscillator to create a modulated RF output;

means for comparing said modulated RF output to a reference frequency input to create a phase error signal; and

5 means for lowpass filtering said phase error signal to produce said loop control signal in order to reduce the effects of said modulation control signal on said loop control signal.

8. The system of generating a radio frequency spread spectrum signal of Claim 7 further comprising means for generating said digital direct sequence spread spectrum waveform using a spreading sequence which has a very low spectral energy at or near 0 Hz.

10 9. A system for receiving a spread spectrum signal comprising:

an analog to digital converter receiving an in-phase baseband component of a received signal and producing in-phase digital data;

an analog to digital converter receiving a quadrature baseband component of said received signal and producing quadrature digital data;

15 a frequency shift keying demodulator receiving said in-phase and quadrature digital data and producing demodulated chip data; and

a matched filter receiving said demodulated chip data and producing estimated bit data.

10. A method of demodulating a radio frequency spread spectrum signal comprising the steps of:

20 producing an in-phase baseband component and a quadrature baseband component of said radio frequency spread spectrum signal;

converting said in-phase and quadrature baseband components to an in-phase digital data stream and a quadrature digital data stream respectively;

demodulating said in-phase and quadrature digital data streams to produce a demodulated chip stream; and

25 despread said demodulated chip stream to produce estimated information bit data.

11. A system for demodulating a radio frequency spread spectrum signal comprising:

means for producing an in-phase baseband component and a quadrature baseband component of said radio frequency spread spectrum signal;

30 means for converting said in-phase and quadrature baseband components to an in-phase digital data stream and a quadrature digital data stream respectively;

means for demodulating said in-phase and quadrature digital data streams to produce a demodulated chip stream; and

means for despread said demodulated chip stream to produce estimated information bit data.

DIGITAL
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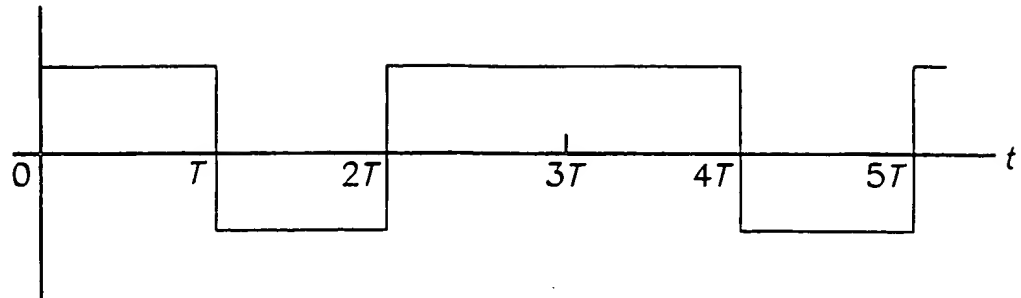


FIG. 1A

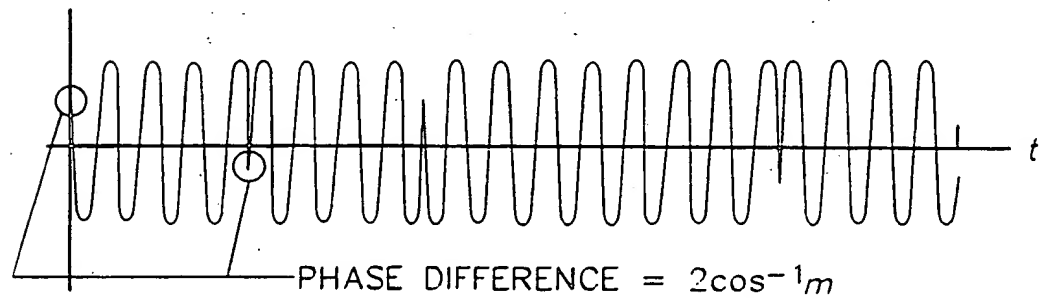


FIG. 1B

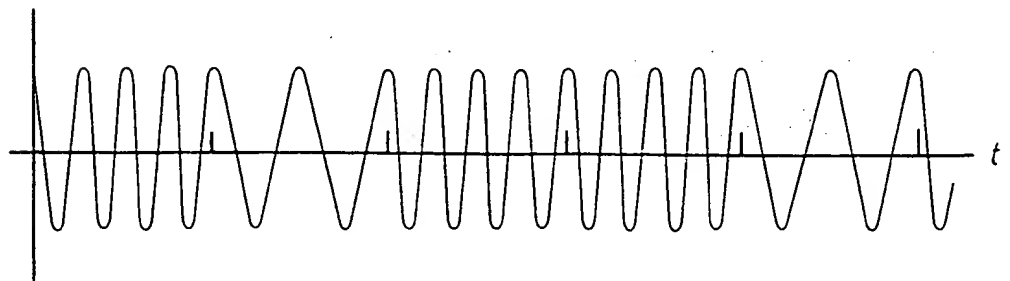


FIG. 1C

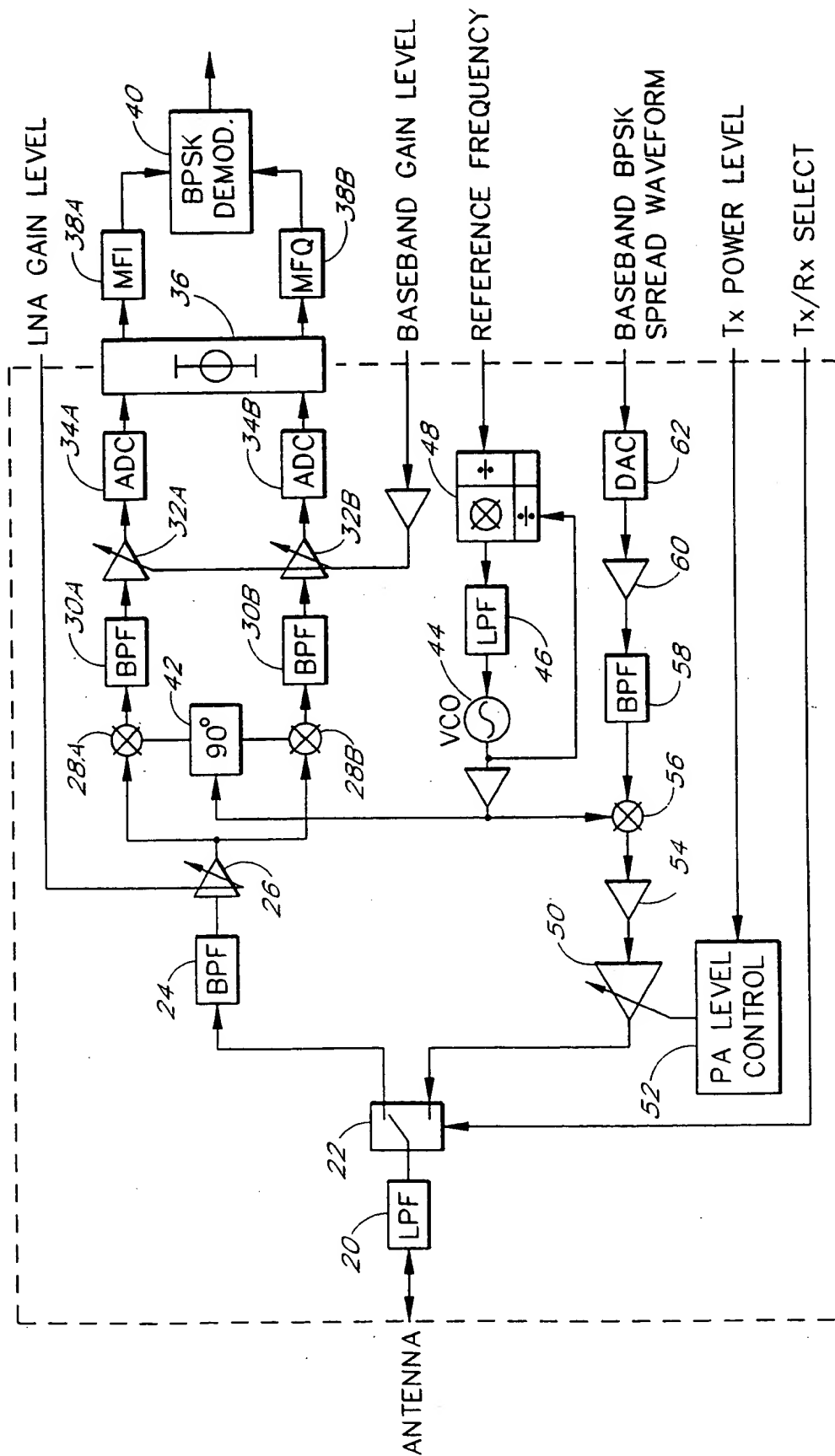


FIG. 2

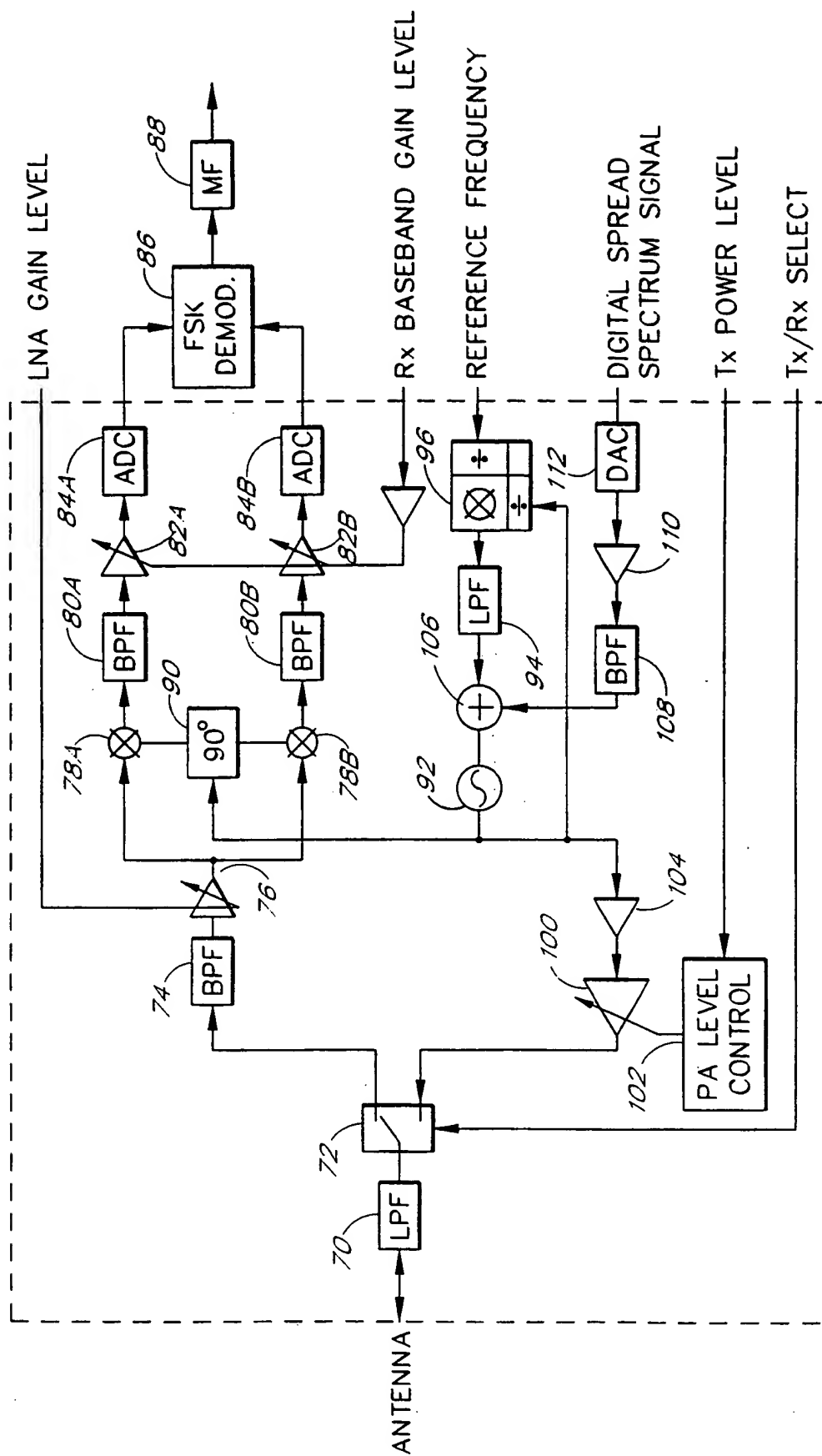


FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/14813

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04B1/40 H04B1/30 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04L H03C H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 027 087 A (ROTTINGHAUS ALAN P) 25 June 1991 (1991-06-25) abstract column 1, line 55 -column 3, line 23 figure 1	1,2,4,5, 7
A	WO 96 32784 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 17 October 1996 (1996-10-17) abstract page 2, line 10 -page 3, line 31 page 5, line 25 -page 8, line 1 figure 4	3,6,8-11
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Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

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Date of the actual completion of the international search

7 October 1999

Date of mailing of the international search report

13/10/1999

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INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 99/14813

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 4 972 430 A (CANTWELL ROBERT H) 20 November 1990 (1990-11-20) abstract column 4, line 49 -column 5, line 19 figure 1 -----	10,11 9

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/14813

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		AU 8851891 A	21-08-1991
		CA 2049346 A,C	03-08-1991
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